Ordering number: EN 3356

CMOS LSI

No. 3356

LC7185-8750

CB Transceiver PLL Frequency Synthesizer and Controller

Overview

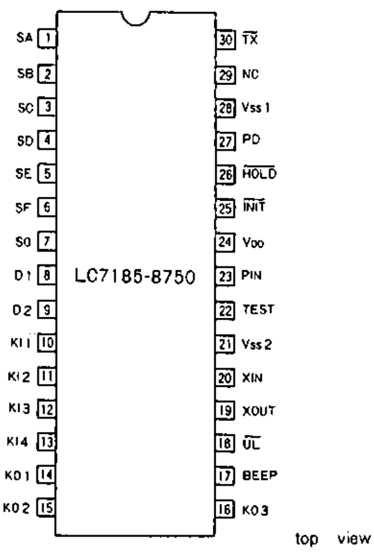
This 27MHz band, PLL frequency synthesizer LSI chip is designed specifically for CB transceivers. The specificaitons are suited for use in U.S.A.(FCC).

The LC7185-8750 incorporates PLL circuitry and a controller for CB applications on a single CMOS chip. The controller handles the PLL circuitry, frequency data ROM, channel preset/recall RAM, and LED display drivers. It also supports channel scan, channel preset/recall, and emergency channel call.

Features

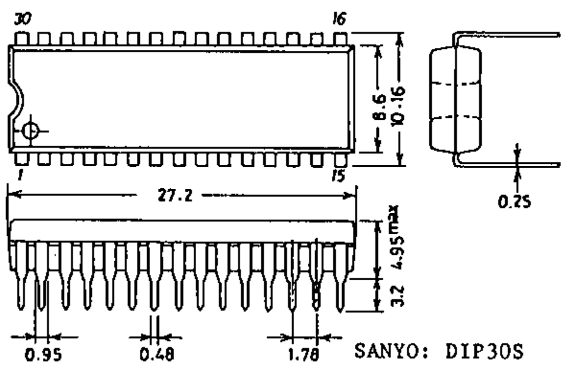
1. A built-in programmable divider for the 16MHz VCO
2. Transmission is inhibited when the PLL is unlocked (digital lock monitor).
3. Direct channel 9 or 19 selection (sliding switch)
4. A 7-segment, 2-character LED display
5. "PA" is displayed in public announcement mode.
6. Output beep-tone control circuitry
7. Up to 5 channel settings can be stored in memory.
8. 4 x 3 key matrix implementation

Pin Assignment



top view

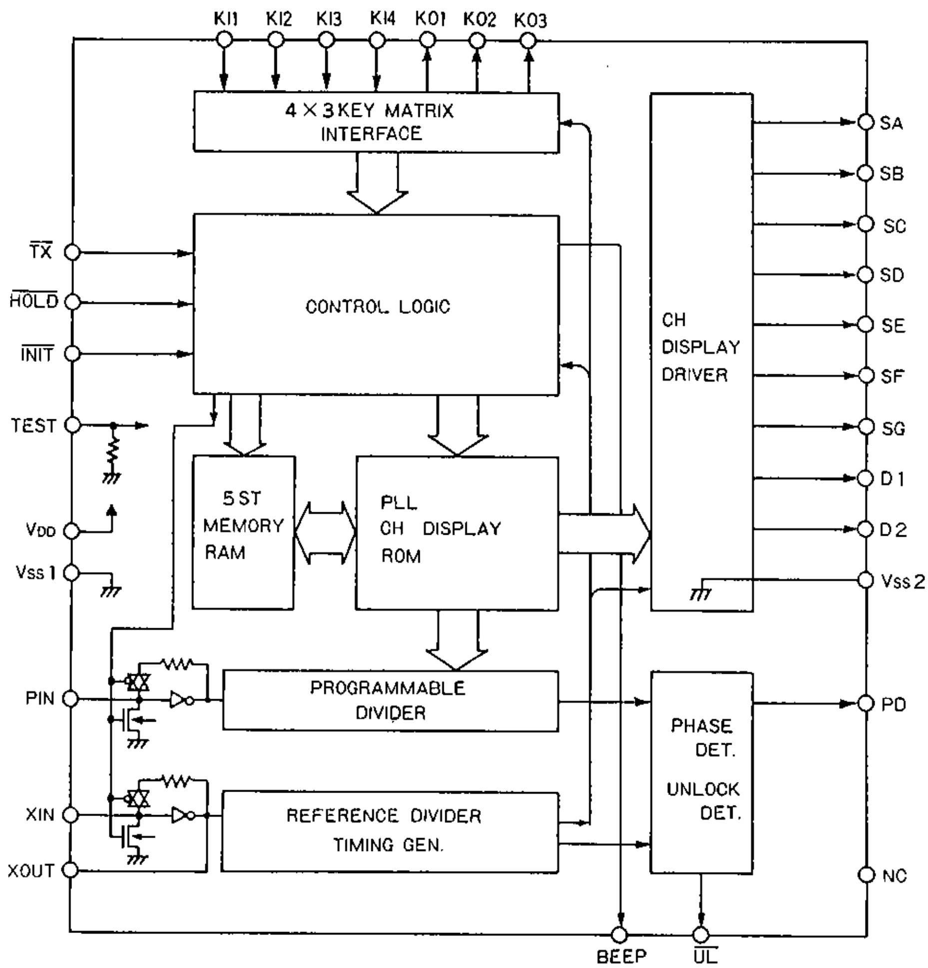
Package Dimensions 3061-D30SNIC
(unit: mm)



SANYO: DIP30S

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10,1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Block Diagram



Pin Descriptions

$\overline{\text{TX}}$:	Transmit/receive select	$\overline{\text{UL}}$:	Unlock detected output
$\overline{\text{HOLD}}$:	Hold mode select	PD:	Charge pump output
$\overline{\text{INIT}}$:	Initial input	NC:	NC pin
TEST:	Test point (input)	SA to SG:	Segment drivers (for display)
V_{DD}, V_{SS1}, V_{SS2}:	Power supply	D1,D2:	Digit output (for display)
PIN:	Programmable divider input	KI1 to 4:	Key inputs
XIN,XOUT:	Crystal oscillator input, output (e.g. 10.240MHz)	KO1 to 3:	Key scan outputs
		BEEP:	Beep-tone control output

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

				unit
Maximum Supply Voltage	V_{DD} max	Pin V_{DD}	−0.3∼+9.0	V
Input Voltage	$V_{IN}(1)$max	Pins $\overline{\text{HOLD}}$, $\overline{\text{TX}}$	−0.3∼+15	V
	$V_{IN}(2)$max	Input pins other than $V_{IN}(1)$max	−0.3∼V_{DD}+0.3	V
Output Voltage	$V_O(1)$max	Pins SA,SB,SC,SD,SE,SF,SG,D1,D2	−0.3∼+15	V
	$V_O(2)$max	Pins $\overline{\text{UL}}$,BEEP	−0.3∼+15	V
	$V_O(3)$max	Pin PD	−0.3∼V_{DD}+0.3	V
	$V_O(4)$max	Output pins other than mentioned above	−0.3∼V_{DD}+0.3	V
Output Current	$I_O(1)$max	Pins SA,SB,SC,SD, SE,SF,SG	0∼+30	mA
	$I_O(2)$max	Pins D1,D2	0∼+10	mA
	$I_O(3)$max	Pin $\overline{\text{UL}}$	0∼+20	mA
	$I_O(4)$max	Pin BEEP	0∼+10	mA
Allowable Power Dissipation	Pd max	(Ta≦85°C)	350	mW
Operating Temperature	Topr		−40∼+85	°C
Storage Temperature	Tstg		−55∼+125	°C

Allowable Operating Conditions at Ta=-40 to +85°C, V_{SS}=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		5.0		8.0	V
"H"-Level Input Voltage	$V_{IH}(1)$	Pins $\overline{\text{HOLD}}$,$\overline{\text{TX}}$	0.7V_{DD}		12	V
	$V_{IH}(2)$	Pin $\overline{\text{INIT}}$	3.2		V_{DD}	V
	$V_{IH}(3)$	Pins KI1,KI2,KI3,KI4	0.6V_{DD}		V_{DD}	V
"L"-Level Input Voltage	$V_{IL}(1)$	Pins $\overline{\text{HOLD}}$, $\overline{\text{TX}}$	0		0.3V_{DD}	V
	$V_{IL}(2)$	Pin $\overline{\text{INIT}}$	0		1.3	V
	$V_{IL}(3)$	Pins KI1, KI2, KI3, KI4	0		0.4V_{DD}	V
Output Voltage	$V_{OUT}(1)$	Pins SA, SB, SC, SD, SE, SF, SG, D1, D2	0		13	V
	$V_{OUT}(2)$	Pins $\overline{\text{UL}}$, BEEP	0		8	V
Input Frequency	$f_{IN}(1)$	Pin XIN (sine wave, capacitor coupled)	1.0	10.24	15	MHz
	$f_{IN}(2)$	Pin PIN (sine wave, capacitor coupled)	10		30	MHz
Input Amplitude	$V_{IN}(1)$	Pin XIN (sine wave, capacitor coupled)	0.5		1.5	Vrms
	$V_{IN}(2)$	Pin PIN (sine wave, capacitor coupled)	0.15		1.5	Vrms
Required Oscillating Frequency	X'tal	Pins XIN,XOUT (CI≦50Ω)	5.0	10.24	15	MHz

Electrical Characteristics at under allowable operating conditions

				min	typ	max	unit
Internal Feedback Resistance	Rf(1)	Pin XIN			1.0		MΩ
	Rf(2)	Pin PIN			500		kΩ
Pull-down Resistor	RpdN	Pins KI1,KI2,KI3,KI4, TEST		30	50	70	kΩ
"H"-Level Input Current	$I_{IH}(1)$	Pins $\overline{\text{HOLD}}$,$\overline{\text{TX}}$	V_I=12V			5.0	μA
	$I_{IH}(2)$	Pin $\overline{\text{INIT}}$	V_I=V_{DD}			5.0	μA
	$I_{IH}(3)$	Pin XIN	V_I=V_{DD}			25	μA
	$I_{IH}(4)$	Pin PIN	V_I=V_{DD}			50	μA
"L"-Level Input Current	$I_{IL}(1)$	Pins $\overline{\text{HOLD}}$, $\overline{\text{TX}}$	V_I=Vss			5.0	μA
	$I_{IL}(2)$	Pin $\overline{\text{INIT}}$	V_I=Vss			5.0	μA
	$I_{IL}(3)$	Pin XIN	V_I=Vss			25	μA
	$I_{IL}(4)$	Pin PIN	V_I=Vss			50	μA
"H"-Level Output Voltage	$V_{OH}(1)$	Pins KO1,KO2,KO3	I_O=1mA	V_{DD}−2.0	V_{DD}−1.0	V_{DD}−0.5	V
	$V_{OH}(2)$	Pin PD	I_O=0.5mA	V_{DD}−1.0			V

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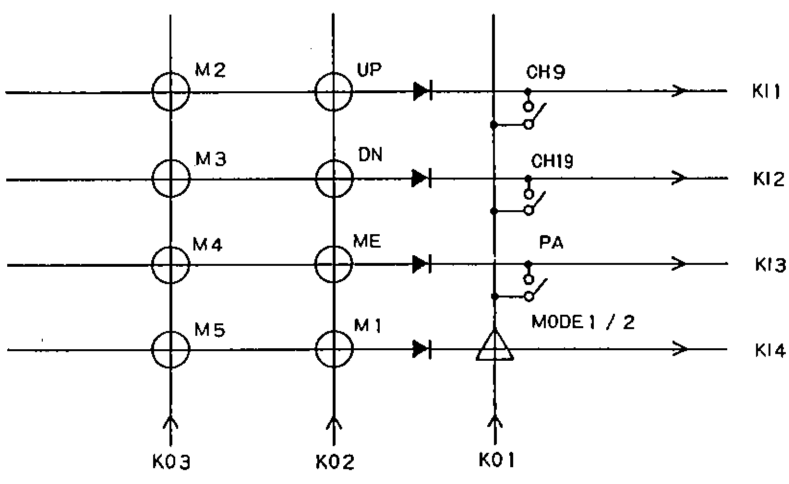
				min	typ	max	unit
"L"-Level Output Voltage	$V_{OL}(1)$	Pins KO1,KO2,KO3	$I_O=20\mu A$	0.6	1.0	1.4	V
	$V_{OL}(2)$	Pin PD	$I_O=0.5mA$			1.0	V
	$V_{OL}(3)$	Pin BEEP	$I_O=2mA$			1.0	V
	$V_{OL}(4)$	Pins SA,SB,SC,SD,SE,SF,SG	$I_O=20mA$			1.0	V
	$V_{OL}(5)$	Pins D1,D2	$I_O=5mA$			1.0	V
	$V_{OL}(6)$	Pin $\overline{UL}$	$I_O=10mA$			1.0	V
Output Leakage Current	$I_{OFF}(1)$	Pins SA,SB,SC,SD,SE,SF,SG				5.0	μA
		Pins D1,D2	$V_O=13V$			5.0	μA
	$I_{OFF}(2)$	Pins $\overline{UL}$,BEEP	$V_O=8V$			5.0	μA
"H"-Level Tristate Leakage Current	I_{OFFH}	Pin PD	$V_O=V_{DD}$		0.01	10.0	nA
"L"-Level Tristate Leakage Current	I_{OFFL}	Pin PD	$V_O=V_{SS}$		0.01	10.0	nA
Supply Current	$I_{DD}(1)$	Normal mode ※1 (PLL operates)			5	10	mA
	$I_{DD}(2)$	Hold mode ※2 (memory backup)	$V_{DD}=3.0V$			5	μA
			$V_{DD}=8.0V$			15	μA

※1: $f_{IN}(2)=20MHz$ (PIN)
$V_{IN}(2)=0.15Vrms$
X'tal=10.240MHz
$\overline{TX}=\overline{HOLD}=\overline{INIT}=V_{DD}$
Other inputs $=V_{SS}$
Other outputs = open

※2: $\overline{HOLD}=V_{SS}$
$\overline{TX}=\overline{INIT}=V_{DD}$
Other inputs $=V_{SS}$
Other outputs = open

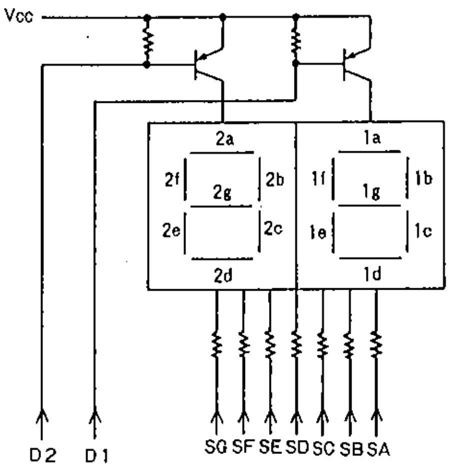
Note: Be careful that the dielectric strength of pins SA, SB, SC, SD, SE, SF, D1, D2, UL, BEEP are weak.

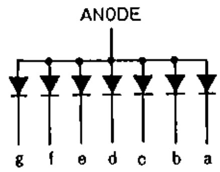
Key Matrix



CH9	: Emergency CH9 recall	UP / DN / ME / M1~5	: Momentary SW
CH19	: Emergency CH19 recall	CH9 / CH19 / PA	: Slide SW
PA	: Public announcement display	MODE1 / 2	: Diode
MODE1 / 2	: Display Mode		
UP	: CH up / scan		
DN	: CH down / scan		
ME	: Station Memory Enable		
M1 ~M5	: Station Memory recall		

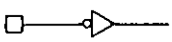
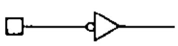
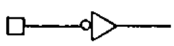
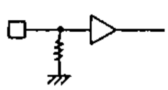
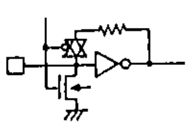
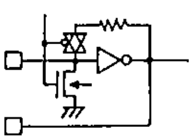
LED Display Configuration (Common anode/7 segment)





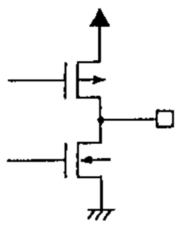
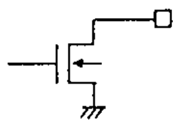
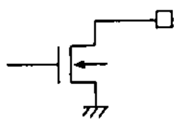
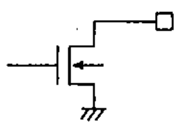
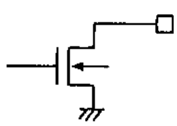
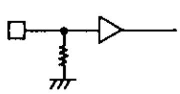
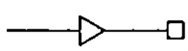
	SG	SF	SE	SD	SC	SB	SA
D1	1g	1f	1e	1d	1c	1b	1a
D2	2g	2f	2e	2d	2c	2b	2a

Pin Description

Pin Name	Pin No.	Type	Description
$\overline{TX}$	30		• Transmit/receive select $\overline{TX}$="0"...Transmit, TX="1"...Receive
$\overline{HOLD}$	26		• Hold mode select $\overline{HOLD}$="0"...Hold mode select ="1"...Normal mode select
$\overline{INIT}$	25		• Reset line $\overline{INIT}$="0"...Reset
TEST	22		• Test point (input) Tie to ground or leave floating
VDD	24		• Power supply (+) Normal mode: 5.0 to 8.0V Hold mode: ≥3.2V
Vss 2	21		• Channel display LED driver ground
PIN	23		• Programmable divider input 150mVrms min Hold mode: Programmable divider is disabled.
XIN XOUT	20 19		• Crystal oscillator Frequency: 10.24MHz Hold mode: Oscillator is disabled.

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Pin Name	Pin No.	Type	Description
PD	27		• Charge pump output from the phase comparator - fV is obtained by dividing the PIN frequency input by N (programmable divider value) - fR is the reference signal (reference divider output) fV>fR OR leading: Positive Pulses fV<fR OR leading: Negative Pulses fV=fR and phase muched: High impedance Hold mode: High impedance
Vss 1	28		• PLL circuit and controller ground
NC	29		• No-connection
$\overline{UL}$	18		• Unlock detected output Low level: See Unlock Detected Output (UL) for detail. Open: Locked
BEEP	17		• Beep-tone control output Open: See Beep-tone Control Output for detail. Low level: Hold mode.
SA to SG	1 to 7		• Segment drivers for the display (Common anode/7 segments)
D1 D2	8 9		• Digit output (150Hz) for the display (Common anode/7 segments) Hold mode: Tr goes off.
KI1 to KI4	10 to 13		• Key inputs Input from the key matrix
KO1 to KO3	14 to 16		• Key scan output (75Hz) Output to the key matrix Hold mode: Low (scanning stops)

Operation

(1) Channel Selection (up/down)

The unlock detected line ($\overline{UL}$) is asserted (low) when the UP (or DN) key is pressed and deactivated 25ms after the key is released (see diagram below).

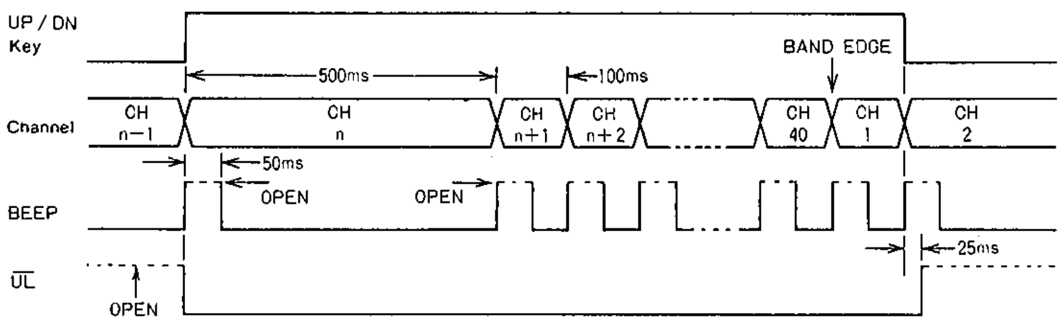
The beep-tone control line (BEEP) is asserted (open) for 50ms after each new channel is selected (see diagram below).

1) Manual scanning (up/down)

Pressing the UP key increments by one channel and pressing the DN key decrements by channel. When scanning reaches the end of the band, it automatically wraps around to the beginning.

2) Auto scanning (up/down)

Holding the UP (or DN) key down for 500ms or longer starts auto scanning. For both up and down scanning, each channel takes 100msec to scan.



(2) Selecting an Emergency Channel (CH9/CH19)

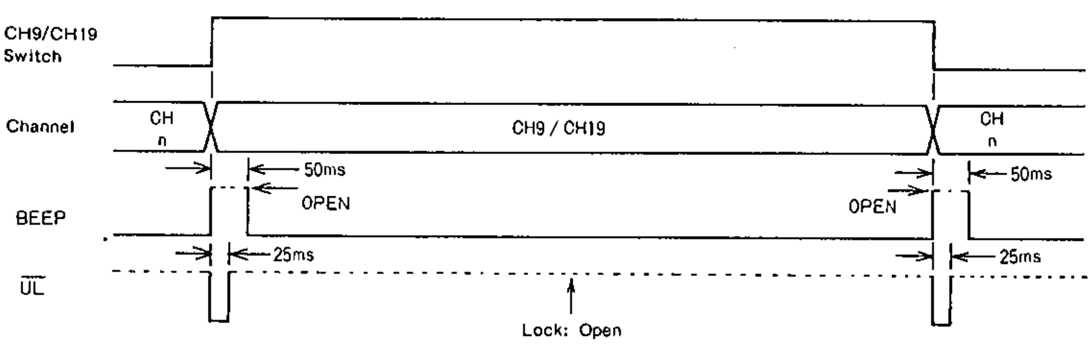
If the CH9 or CH19 switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Asserts the beep-tone control line for 50ms
- Disables the UP/DN, M1 to M5, and ME switches
- Causes either "9" or "19" to blink on the display
- Keep the emergency channel open until the CH9 or CH19 switch is turned off.

After the CH9 or CH19 switch is turned back off the beep-tone control line is asserted for 50ms and the LC7185 reopens the previous channel.

Note the CH9 has a higher priority over CH19. As a result, if both switches are turned on, CH9 will be opened.

As shown in the diagram, the $\overline{UL}$ line is asserted for 25ms after the CH9 or CH19 switch is turned off or on.

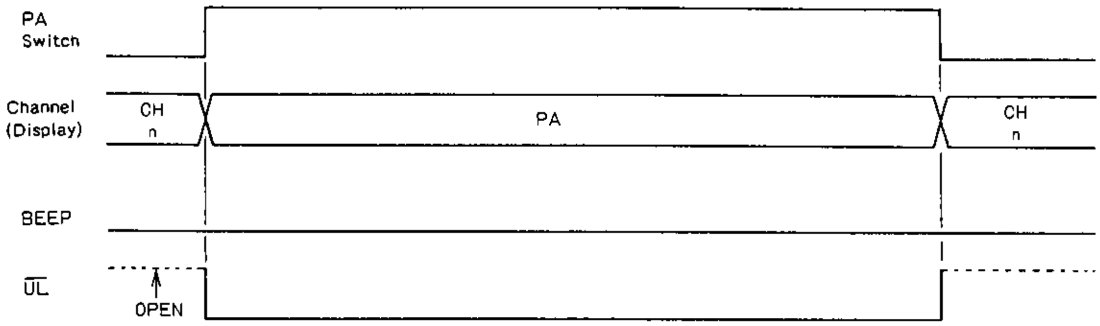


(3) Public Announcement (PA) Mode

When the PA switch is turned on, the LC7185 does the following:

- Stores the value of the previous channel
- Disables all keys
- Causes "PA" to be displayed
- Stays in PA mode until the PA switch is turned off.

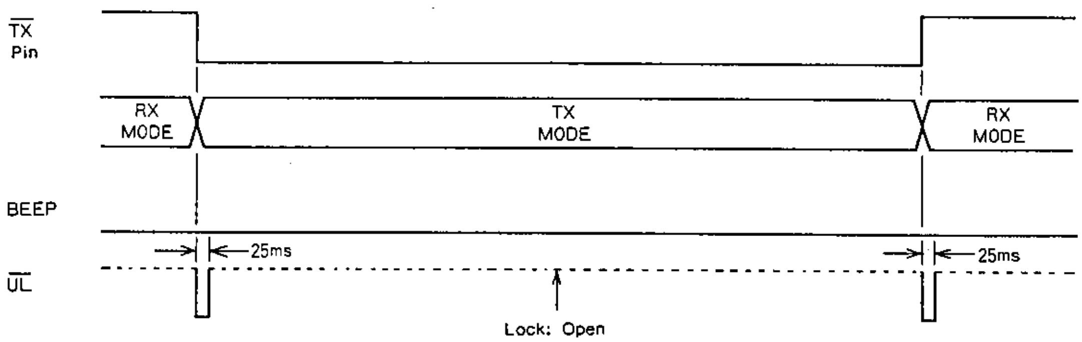
When the PA switch is turned back off, the LC7185 leaves PA mode and reopens the previous channel. As shown in the diagram, the $\overline{\text{UL}}$ line is asserted while the PA switch is turned on.



(4) Transmit/Receive Selection

When the $\overline{\text{TX}}$ line is asserted, the LC7185 enters TX mode. The LC7185 will only leave this mode if the PA switch is pressed or the $\overline{\text{TX}}$ line is deactivated.

As shown in the diagram, the $\overline{\text{UL}}$ line is asserted for 25ms after the TX line is asserted or deactivated.



(5) Channel Preset/Recall Facility

1. The LC7185 allows up to 5 channels to be preset (assigned to M1 to M5).
   - After a reset, M1 to M5 are assigned to CH33.
2. Recalling preset channels
   - A preset channel is recalled by pressing one of the preset memory keys (M1 to M5)* to which the channel was previously assigned.
   - Presetting channel (assigning keys) are covered in the next section. There are two different display modes as shown below.

Mode 1 (without diode)

Each time a key is pressed (e.g. M1), the new channel is displayed.

Example: Display 21 → 15
Key M1

Mode 2 (with diode)

Each time a key is pressed (e.g. M1), a key mnemonic (e.g. "P1") is displayed for 400msec, then the new channel is displayed.

Example: Display 21 → P1 → 15
400ms
Key M1

3. Presetting channels

Presetting a channel is done in the following way. First select the channel to be preset, then hold down the ME key and press the preset memory key (M1 to M5)* to which you would like to assign the current channel.

In the following cases, a channel will not be preset:

- 9 seconds elapse after the ME key is pressed and one of M1 to M5 is pressed.
- Emergency channels CH9 or CH19 are currently selected.
- The $\overline{TX}$ line is asserted.
- The PA switch is turned on (PA mode).
- The $\overline{HOLD}$ line is asserted (hold mode).

There are two different display modes as shown below.

Mode 1 (without diode)

The current channel is displayed throughout the preset process.

Example: Display 15 ⟶ 15

Key [ME] [M1]

Mode 2 (with diode)

When the ME key is held down, "PE" is flashed on the display. Once a preset memory key is pressed (e.g. M1), the key mnemonic (e.g. "P1") is displayed for 400msec before the current channel is redisplayed.

Example: Display 15 ⟶ PE ⟶ P1 ⟶ 15

400ms

Key [ME] [M1]

*Note that if two or more keys are pressed at the same time, priority is assigned as follows:

M1>M2>M3>M4>M5

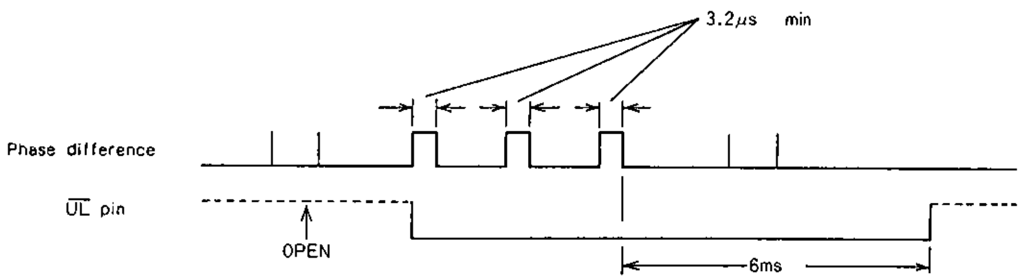
(6) Beep-tone Control Output

After each of the following events, the BEEP line is asserted for 50msec:

- A reset (e.g. battery replacement)
- Any key press associated with the channel memory
- Any emergency channel switch activation
- A new channel is selected
- Leaving hold mode

(7) Unlock Detected Output ($\overline{UL}$)

In the following cases, the $\overline{UL}$ line is asserted for the duration indicated.

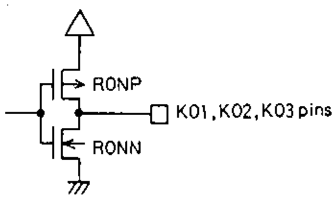


- When the phase difference between the programmable and reference divider outputs exceeds 3.2μs . The $\overline{UL}$ line is held low for 6ms after the last out-of-range phase sample is detected, as shown below.
- After a new transmit/receive or channel selection. The $\overline{UL}$ line is asserted for 25ms .
- While the PA switch is turned on.

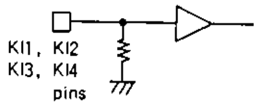
(8) Key Matrix

It is normal to put diodes in series with the key scanning lines to avoid creating a short with the output lines.

But K01, K02 and K03 lines don't need diodes.



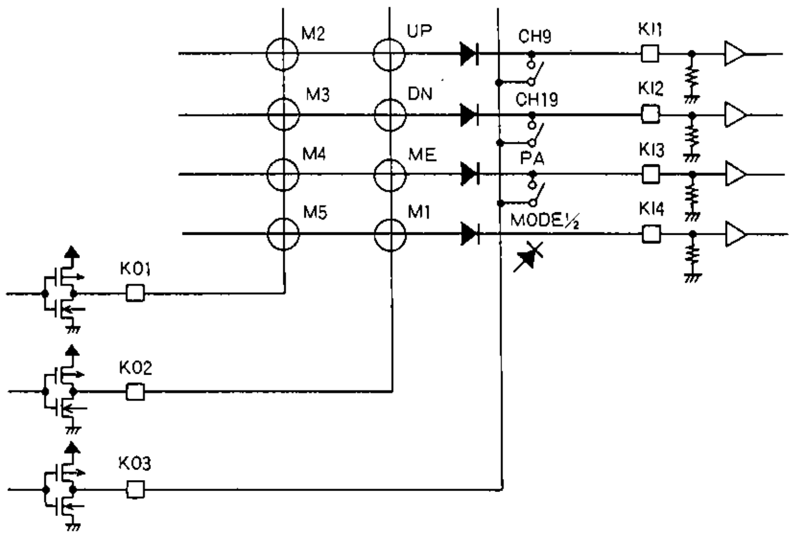
RONP, RONN : On impedance



RpdN : Pull-down resistor

unit : kΩ

Item	min	typ	max
RONP	0.5	1.0	2.0
RONN	30	50	70
RpdN	30	50	70



Hold Mode

The LC7185 enters hold mode when the $\overline{\text{HOLD}}$ line is asserted. In this mode, the channel preset/recall RAM is not affected.

(1) System Status

The LC7185 will remain in hold mode until the $\overline{\text{HOLD}}$ line is deactivated or a reset occurs ($\overline{\text{INIT}}$ line is asserted). The programmable divider, crystal oscillator, and reference divider are all inhibited. Signal output levels are shown below.

PD: High impedance

$\overline{\text{UL}}$: Vss (ground)

D1, D2: High impedance

BEEP: Vss

K01 to K03: Vss

When the LC7185 leaves hold mode, the previously selected channel is reopened.

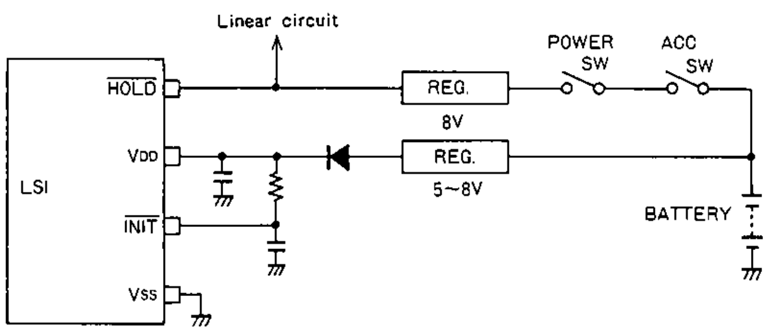
(2) Reset

To reset the chip, assert the $\overline{\text{INIT}}$ line,

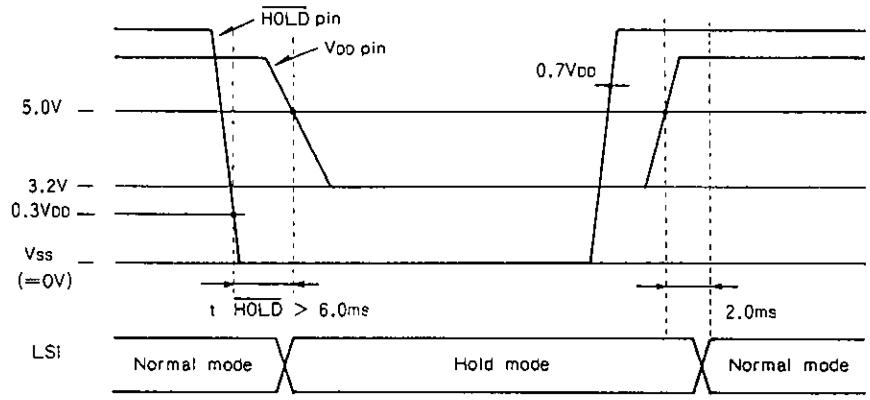
Reset state:

•CH9 is selected.

•Preset memory keys are all set to CH33.



(3) Timing Requirements for Hold Mode



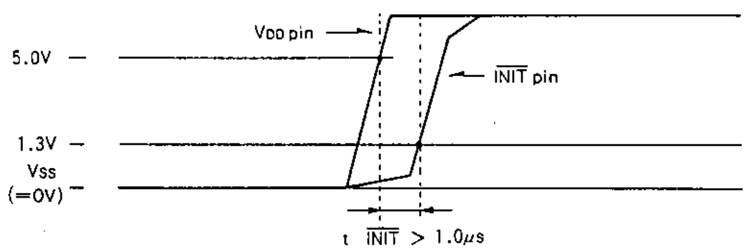
V_{DD} must remain at 5.0V or higher (crystal oscillator requirement) for 6.0msec (tHOLD) after the HOLD line is asserted (HOLD<0.3V_{DD}). After this V_{DD} may go as low as 3.2V. There are no constraints on timing when the chip is leaving hold mode.

The signals can be activated in one of two orders.

1) If HOLD is already deactivated (>0.7V_{DD}), the LC7185 leaves hold mode within 2.0msec after V_{DD} rises to >5.0V.
2) If V_{DD} is >5.0V, the LC7185 enters normal mode within 2.0ms after HOLD is deactivated.

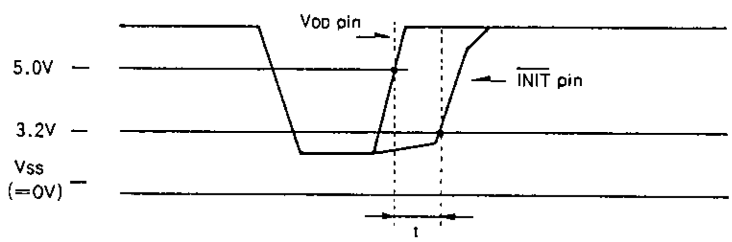
(4) Reset Timing

1) Reset timing (e.g. battery replacement)



Note: $t_{\overline{INIT}}$ should be greater than 1.0μs .

2) Reset caused by a sudden voltage (V_{DD}) drop



Note: If V_{DD} drops momentarily down to less than 3.0V and rises up to more than 5.0V (t>1.0μs), a reset may be generated.

Frequency Table (U.S.A.; LC7185-8750)

CHANNEL	FREQUENCY (MHz)	RX ($\overline{TX}$=1)		TX ($\overline{TX}$=0)	
		N	Fvco	N	Fvco
1	26.965	6508	16.27	5393	13.4825
2	26.975	6512	16.28	5395	13.4875
3	26.985	6516	16.29	5397	13.4925
4	27.005	6524	16.31	5401	13.5025
5	27.015	6528	16.32	5403	13.5075
6	27.025	6532	16.33	5405	13.5125
7	27.035	6536	16.34	5407	13.5175
8	27.055	6544	16.36	5411	13.5275
9	27.065	6548	16.37	5413	13.5325
10	27.075	6552	16.38	5415	13.5375
11	27.085	6556	16.39	5417	13.5425
12	27.105	6564	16.41	5421	13.5525
13	27.115	6568	16.42	5423	13.5575
14	27.125	6572	16.43	5425	13.5625
15	27.135	6576	16.44	5427	13.5675
16	27.155	6584	16.46	5431	13.5775
17	27.165	6588	16.47	5433	13.5825
18	27.175	6592	16.48	5435	13.5875
19	27.185	6596	16.49	5437	13.5925
20	27.205	6604	16.51	5441	13.6025
21	27.215	6608	16.52	5443	13.6075
22	27.225	6612	16.53	5445	13.6125
23	27.255	6624	16.56	5451	13.6275
24	27.235	6616	16.54	5447	13.6175
25	27.245	6620	16.55	5449	13.6225
26	27.265	6628	16.57	5453	13.6325
27	27.275	6632	16.58	5455	13.6375
28	27.285	6636	16.59	5457	13.6425
29	27.295	6640	16.60	5459	13.6475
30	27.305	6644	16.61	5461	13.6525
31	27.315	6648	16.62	5463	13.6575
32	27.325	6652	16.63	5465	13.6625
33	27.335	6656	16.64	5467	13.6675
34	27.345	6660	16.65	5469	13.6725
35	27.355	6664	16.66	5471	13.6775
36	27.365	6668	16.67	5473	13.6825
37	27.375	6672	16.68	5475	13.6875
38	27.385	6676	16.69	5477	13.6925
39	27.395	6680	16.70	5479	13.6975
40	27.405	6684	16.71	5481	13.7025

Vco (TX) = RF ÷ 2

Vco (RX) = RF − 10.695 MHz (IF)

CH 1 : Vco (TX) = 26.965 ÷ 2 = 13.4825

Vco (RX) = 26.965 − 10.965 = 16.27

Sample Application Circuit

